12.7 A 15mW 0.2mm² 10b 50MS/s ADC with Wide Input Range

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As the recent wireless communication systems have converged with mobile broadcasting systems, such as DVB-H, DVB-T, Satellite DMB (SDMB), and Terrestrial DMB (TDMB), low power consumption and small size become one of the significant requirements for mobile SoC applications. The ADCs for such applications usually need to have input bandwidths of up to 38MHz and input dynamic range of greater than $1.5V_{pp}$. The conventional deep sub-micron CMOS ADCs are typically implemented with dual gate-oxide (DGOX) transistors using a nominal gate voltage of 2.5V or 3.3V at the expense of larger area and more power. To achieve low power and small area in the proposed ADC, the entire ADC except an analog input sampling network is designed with single gate-oxide (SGOX) short-channel transistors exploiting low supply voltage of 1.2V. Only the analog input sampling network of the ADC that includes gate bootstrapping [1] is implemented with DGOX transistors that operate from a 2.7V supply and sample a wide dynamic range analog input of up to $2V_{pp}$ at the Nyquist rate.

The proposed 10b 50MS/s ADC uses a 2.8b/stage pipelined architecture and consists of a high-to-low level-shifting SHA, four multiplying DACs (MDACs), five flash ADCs, and other supplementary blocks, as shown in Fig. 12.7.1. The block diagram of the analog level-shifting SHA and its associated timing diagram are shown Fig. 12.7.1. The dotted rectangle in the SHA represents the analog input sampling network. The SHA operates with two-phase non-overlapping clocks denoted as Q1 and Q2; the sampling and the amplification phase, respectively. The Q1H and Q2H, low-to-high level-shifted clocks of Q1 and Q2, are applied to the gate of DGOX devices. The $2V_{pp}$ input signal sampled by an input sampling network is reduced to $1V_{pp}$ by choosing $C_F=2C_S$ for 1.2V operation.

The schematic diagram of the opamp used in the SHA and MDACs is shown in Fig. 12.7.2. Because opamps are the most power-consuming analog blocks in the pipelined ADC, an improved compensation technique [2] and a partially switched opamp technique [3] are adopted to minimize the current of opamps. During the sampling phase, switch transistors M3, M4, and M7 are off. At the same time, both differential outputs, OUT+ and OUT-, are connected to VCOM through M5 and M6 and the gate of M9 is connected to the VB5 by M8 for achieving fast settling of the opamp in the next phase. The T1 node is set by turning on M7 before amplification begins. During the amplification phase, switch transistors M3 and M4 are on to amplify the input signal. The timing difference between M7 and M3 (M4) is to reduce the power consumption of the opamp without settling time degradation. A modified CMFB block is adopted in the second stage opamp, as shown in Fig. 12.7.2. The proposed dynamic CMFB circuit, referred to as CMFB2, is composed of only two capacitors and three switches, that is, half the number of elements of the conventional CMFB [4]. The proposed CMFB is optimized for this open loop sampling architecture that resets the opamp during the sampling phase. Incorporating the proposed opamp, the power consumption and chip area of the ADC are reduced by about 30% as compared to the conventional ADCs.

For low-voltage operation it is important to have a PVT-insensitive bias voltage for the opamp. Figure 12.7.3 shows the schematic diagram of such a bias generator. The proposed bias generator is composed of a start-up, a current-reference circuit, and an amp bias circuit. In the supply-independent current-reference circuit, long channel transistor M3 is added to the conventional current-reference circuit [5] to compensate for the variation of I_{REF} due to the channel-length modulation of M1 and M5, which is in proportion to the supply voltage variation. To achieve wide-signal-swing range with a low-supply voltage, it is important to make the voltage differences VB_{12} (=VB1-VB2) and VB_{34} (=VB3-VB4) to be constant. However, it is difficult for the opamp to operate stably with enough swing margin because VB_{12} and VB_{34} are sensitive to PVT variations. VB_{12} and VB_{34} are determined by I_{REF}, which is inversely proportional to the square of R1 in the current-reference circuit. Therefore, the amp bias circuit uses the same resistor type, used in the current-reference circuit to minimize the sensitivity of the bias voltage to the resistance variation. Consequently, sufficient opamp margin can be acquired regardless of PVT variations. The low-voltage opamp with the proposed biasing technique operates from a supply voltage of 0.9V to 1.5V.

The prototype ADC is fabricated in a 0.13μm single-poly five-metal CMOS process. It consumes 15mW at 50MS/s from 1.2V and 2.7V power supplies. The active die area is 0.2mm² (=590μm×340μm), as shown in Fig. 12.7.4. The 2.7V supply is only applied to the devices in the dotted rectangle and the power consumption of the block is 7% of the total power consumption of the ADC. The performance plots of the ADC are shown in Fig. 12.7.5. The measured DNL and INL are ±0.17LSB and ±0.16LSB, respectively. At a clock frequency of 50MHz, the measured SNDR and SFDR are 57.2dB and 72.9dB for the Nyquist input, and 56.6dB and 70.4dB for 50MHz input, respectively. The SNDR, THD, and SFDR versus the sampling frequency for 5MHz input are plotted in Fig. 12.7.6. The SNDR maintains better than 55dB up to 80MS/s. The overall ADC performance is summarized in Fig. 12.7.7.

References:

[1] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipelined Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May, 1999.

[2] B. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 629-633, Dec., 1983.

[3] H. C. Kim, D. K. Jeong, and W. C. Kim, "A 30mW 8b 200MS/s Pipelined CMOS ADC Using a Switched-Opamp Technique," *ISSCC Dig. Tech. Papers*, pp. 284-285, Feb., 2005.

[4] R. Castello and P. Gray, "A High-Performance Micropower Switched-Capacitor Filter," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1122-1132, Dec., 1985.

[5] M. J. Kim, H. S. Yoon, Y. J. Lee, and S. H. Lee, "An 11b 70MHz 1.2mm² 49mW 0.18μm CMOS ADC with On-Chip Current/Voltage References," *ESSCIRC,* pp. 463-466, Sept., 2002.

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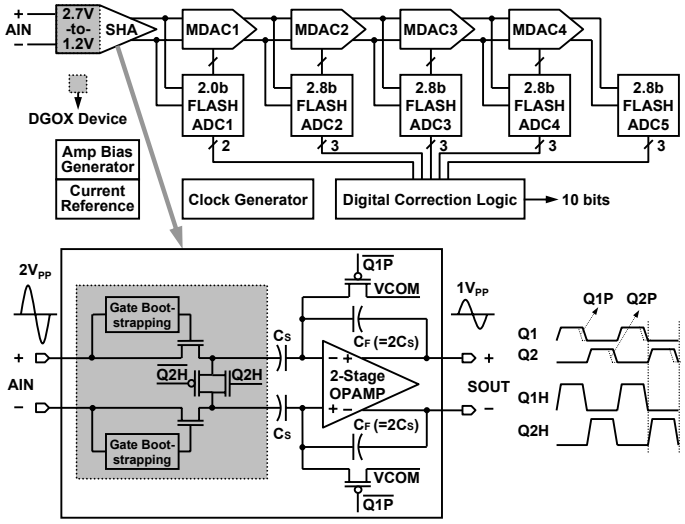

Figure 12.7.1: Block diagram of the proposed ADC with analog level-shifting SHA.

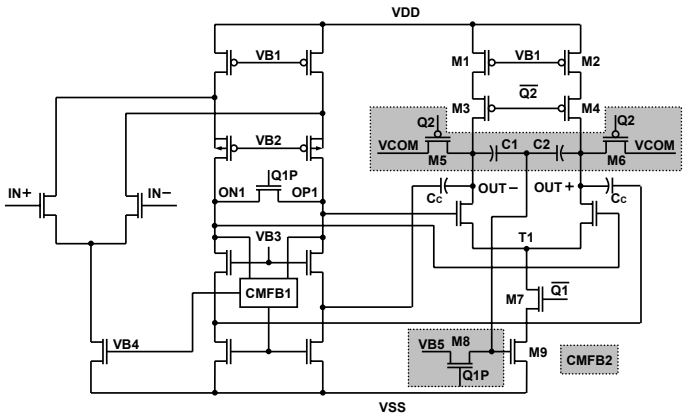

Figure 12.7.2: Two-stage switched opamp.

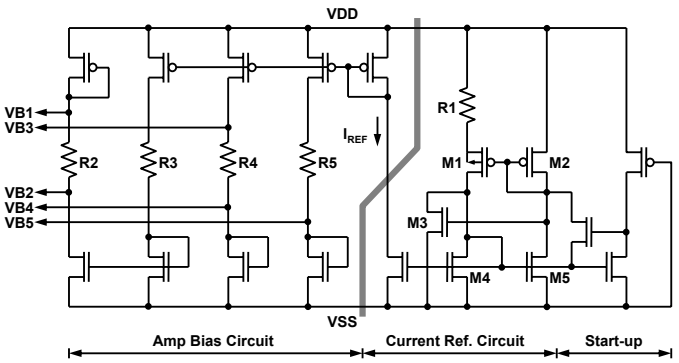

Figure 12.7.3: Proposed PVT-insensitive bias generator.

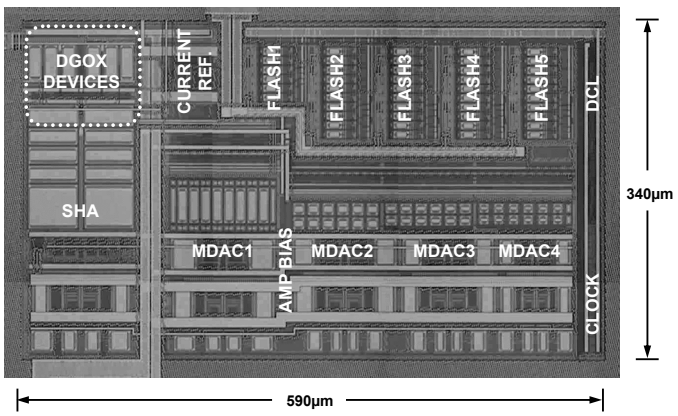

Figure 12.7.4: Die micrograph of the ADC (590μm×340μm).

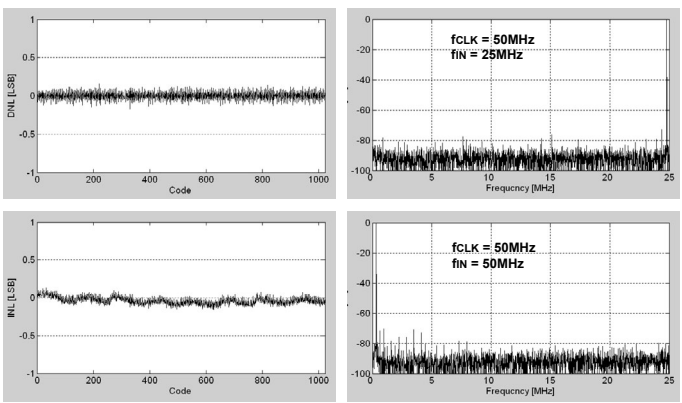

Figure 12.7.5: Measured INL, DNL, and FFT spectrums.

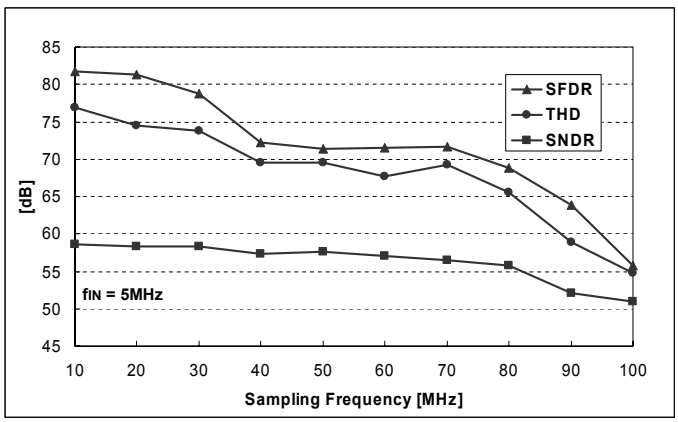

Figure 12.7.6: Measured THD, SNDR, and SFDR.

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Resolution	10 bits
Conversion Rate	50MS/s
Process	0.13μm 1 poly 5 metal CMOS
Supply Voltage	1.2V / 2.7V
Input Range	$2V_{pp}$
DNL / INL	± 0.17LSB / ± 0.16LSB
SNDR/SFDR (@ f_{IN} = 25MHz)	57.2dB / 72.9dB
SNDR/SFDR (@ f_{IN} = 50MHz)	56.6dB / 70.4dB
Power Dissipation	15mW
Active Die Area	$0.2mm^2$ (=590μm × 340μm)

Figure 12.7.7: Performance summary of the proposed ADC.

